

WHAT IS CLAIMED IS:

1. A method to determine a frequency offset to be applied in a wireless communication device, the method comprising:

averaging a first set of frequency error estimates to determine a short-term average value;

averaging a second set of frequency error estimates to determine a long-term average value, the second set comprising a superset of the first set of frequency error estimates;

determining the frequency offset as a function of the short-term average value when the short-term average value exceeds a short-term threshold value; and

determining the frequency offset as a function of the long-term average value when the long-term average value exceeds a long-term threshold value lower than the short-term threshold value.

2. The method of claim 1, further comprising:

determining an average value of a third set of frequency error estimates, the third set comprising a superset of the second set of frequency error estimates; and

determining the frequency offset as a function of the average value of the third set of frequency error estimates.

3. The method of claim 1, further comprising adjusting an oscillator frequency as a function of the frequency offset.

4. The method of claim 3, wherein adjusting the oscillator frequency comprises writing the frequency offset to a memory associated with an oscillator.

5. The method of claim 1, wherein:

the wireless communication device is configured to detect a frequency control channel (FCCH); and

determining the frequency offset comprises

using one of the short-term average value and the long-term average value as the frequency offset when the one of the short-term average value and the long-term average value exceeds an FCCH error threshold, and

using a value equal to half of the one of the short-term average value and the long-term average value as the frequency offset when the one of the short-term average value and the long-term average value does not exceed the FCCH error threshold.

6. The method of claim 5, further comprising decoding a synchronization channel (SCH) when the one of the short-term average value and the long-term average value is less than an SCH error threshold.

7. The method of claim 1, further comprising decoding at least one of a control channel and a traffic channel.

8. A method to configure an oscillator for use in connection with a wireless communication device, the method comprising:

reading a frequency offset value from a memory associated with the oscillator;

averaging a first set of frequency error estimates to determine a short-term average value;

averaging a second set of frequency error estimates to determine a long-term average value, the second set comprising a superset of the first set of frequency error estimates;

adjusting an oscillator frequency as a function of the short-term average value when the short-term average value exceeds a short-term threshold value; and

adjusting the oscillator frequency as a function of the long-term average value when the long-term average value exceeds a long-term threshold value lower than the short-term threshold value.

9. The method of claim 8, further comprising:

determining an average value of a third set of frequency error estimates, the third set comprising a superset of the second set of frequency error estimates; and

adjusting the oscillator frequency as a function of the average value of the third set of frequency error estimates.

10. The method of claim 8, wherein adjusting the oscillator frequency comprises writing the frequency offset to a memory associated with an oscillator.

11. An integrated circuit (IC) comprising:
an oscillator; and
a processor arrangement operatively coupled to the oscillator and configured to
average a first set of frequency error estimates to determine a short-term
average value,

average a second set of frequency error estimates to determine a long-term
average value, the second set comprising a superset of the first set of frequency error
estimates,

adjust a frequency of the oscillator as a function of the short-term average
value when the short-term average value exceeds a short-term threshold value, and

adjust a frequency of the oscillator as a function of the long-term average
value when the long-term average value exceeds a long-term threshold value lower than the
short-term threshold value.

12. The IC of claim 11, wherein the processor arrangement is further configured
to:

determine an average value of a third set of frequency error estimates, the third set
comprising a superset of the second set of frequency error estimates; and

adjust the frequency of the oscillator as a function of the average value of the third
set of frequency error estimates.

13. The IC of claim 11, further comprising a memory operatively coupled to the
processor arrangement and configured to store a frequency offset to adjust the frequency of
the oscillator.

14. The IC of claim 13, wherein the memory comprises a nonvolatile memory.

15. The IC of claim 11, wherein the processor arrangement is configured to:
detect a frequency control channel (FCCH);

adjust the frequency of the oscillator by one of the short-term average value and the long-term average value when the one of the short-term average value and the long-term average value exceeds an FCCH error threshold; and

adjust the frequency of the oscillator by half of the one of the short-term average value and the long-term average value when the one of the short-term average value and the long-term average value does not exceed the FCCH error threshold.

16. The IC of claim 15, wherein the processor arrangement is configured to decode a synchronization channel (SCH) when the one of the short-term average value and the long-term average value is less than an SCH error threshold.

17. The IC of claim 11, wherein the processor arrangement is configured to decode at least one of a control channel and a traffic channel.

18. A wireless communication device (WCD) comprising:
an antenna arranged to receive an RF signal;
a receive arrangement, operatively coupled to the antenna, to generate a plurality of samples as a function of the RF signal;
an oscillator, operatively coupled to the receive arrangement and configured to generate a frequency; and
a processor arrangement, coupled to receive the plurality of samples from the receive arrangement and configured to
calculate a plurality of frequency error estimates as a function of the samples;
average a first subset of the frequency error estimates to determine a short-term average value,

average a second subset of the frequency error estimates to determine a long-term average value, the second subset comprising a superset of the first subset of frequency error estimates,

adjust the frequency generated by the oscillator as a function of the short-term average value when the short-term average value exceeds a short-term threshold value, and

adjust the frequency generated by the oscillator as a function of the long-term average value when the long-term average value exceeds a long-term threshold value lower than the short-term threshold value.

19. The WCD of claim 18, wherein the processor arrangement is further configured to:

determine an average value of a third set of frequency error estimates, the third set comprising a superset of the second set of frequency error estimates; and

adjust the frequency generated by the oscillator as a function of the average value of the third set of frequency error estimates.

20. The WCD of claim 18, further comprising a memory operatively coupled to the processor arrangement and configured to store a frequency offset to adjust the frequency of the oscillator.

21. The WCD of claim 20, wherein the memory comprises a nonvolatile memory.

22. The WCD of claim 18, wherein the processor arrangement is configured to:
detect a frequency control channel (FCCH);

adjust the frequency of the oscillator by one of the short-term average value and the long-term average value when the one of the short-term average value and the long-term average value exceeds an FCCH error threshold; and

adjust the frequency of the oscillator by half of the one of the short-term average value and the long-term average value when the one of the short-term average value and the long-term average value does not exceed the FCCH error threshold.

23. The WCD of claim 22, wherein the processor arrangement is configured to decode a synchronization channel (SCH) when the one of the short-term average value and the long-term average value is less than an SCH error threshold.

24. The WCD of claim 18, wherein the processor arrangement is configured to decode at least one of a control channel and a traffic channel.

25. A processor arrangement comprising:

means for averaging a first set of frequency error estimates to determine a short-term average value;

means for averaging a second set of frequency error estimates to determine a long-term average value, the second set comprising a superset of the first set of frequency error estimates;

means for adjusting a frequency of the oscillator as a function of the short-term average value when the short-term average value exceeds a short-term threshold value; and

means for adjusting a frequency of the oscillator as a function of the long-term average value when the long-term average value exceeds a long-term threshold value lower than the short-term threshold value.

26. A processor-readable medium containing processor-executable instructions for:

averaging a first set of frequency error estimates to determine a short-term average value;

averaging a second set of frequency error estimates to determine a long-term average value, the second set comprising a superset of the first set of frequency error estimates;

determining a frequency offset as a function of the short-term average value when the short-term average value exceeds a short-term threshold value; and

determining a frequency offset as a function of the long-term average value when the long-term average value exceeds a long-term threshold value lower than the short-term threshold value.

27. The processor-readable medium of claim 26, containing further processor-executable instructions for:

determining an average value of a third set of frequency error estimates, the third set comprising a superset of the second set of frequency error estimates; and

determining the frequency offset as a function of the average value of the third set of frequency error estimates.

28. The processor-readable medium of claim 26, containing further processor-executable instructions for adjusting an oscillator frequency as a function of the frequency offset.

29. The processor-readable medium of claim 28, containing further processor-executable instructions for writing the frequency offset to a memory associated with an oscillator.

30. The processor-readable medium of claim 26, containing further processor-executable instructions for:

detecting a frequency control channel (FCCH);

using one of the short-term average value and the long-term average value as the frequency offset when the one of the short-term average value and the long-term average value exceeds an FCCH error threshold; and

using a value equal to half of the one of the short-term average value and the long-term average value as the frequency offset when the one of the short-term average value and the long-term average value does not exceed the FCCH error threshold.

31. The processor-readable medium of claim 30, containing further processor-executable instructions for decoding a synchronization channel (SCH) when the one of the short-term average value and the long-term average value is less than an SCH error threshold.

32. The processor-readable medium of claim 26, containing further processor-executable instructions for decoding at least one of a control channel and a traffic channel.

33. A processor-readable medium containing processor-executable instructions for:

reading a frequency offset value from a memory associated with an oscillator;

averaging a first set of frequency error estimates to determine a short-term average value;

averaging a second set of frequency error estimates to determine a long-term average value, the second set comprising a superset of the first set of frequency error estimates;

adjusting an oscillator frequency as a function of the short-term average value when the short-term average value exceeds a short-term threshold value; and

adjusting the oscillator frequency as a function of the long-term average value when the long-term average value exceeds a long-term threshold value lower than the short-term threshold value.

34. The processor-readable medium of claim 33, containing further processor-executable instructions for:

determining an average value of a third set of frequency error estimates, the third set comprising a superset of the second set of frequency error estimates; and

adjusting the oscillator frequency as a function of the average value of the third set of frequency error estimates.

35. The processor-readable medium of claim 33, containing further processor-executable instructions for writing the frequency offset to a memory associated with an oscillator.